AMENDMENTS

IN THE SPECIFICATION

Page 4, line 30 - page 5, line 13: Please replace the paragraph with the following paragraph:

As device sizes and features are continually scaled down, however, leakage currents, cross talk and other issues can arise. Limitations in photoresists and other materials and/or techniques utilized in patterning the semiconductor substrate as well as other materials out of which the memory cells are fashioned can, for example, limit the size to which some features, such as wordlines and/or bitlines, can be reduced. One technique to pack more cells into a smaller area is to form the structures closer together. Forming bitlines, for example, closer together shortens the length of the channel defined therebetween. Shortening the channel in such a manner can, however, lead to leakage currents as well as other undesirable performance issues. For example, charge or bit isolation between the two bits stored in the charge trapping layer becomes increasingly difficult as the channel length is decreased and the bits are brought closer together. In this manner, cross-talk can occur, the bits can contaminate one another and operations performed on one bit can affect the other bit (sometimes referred to complimentary bit disturb or CBD). Accordingly, it would be desirable to reduce feature ~~sized~~ sizes so as to increase packing density while mitigating the adverse affects that may result therefrom.

Page 10, lines 17-22: Please replace the paragraph with the following paragraph:

First and second conductive wordlines 418, ~~420~~ 419 are similarly depicted overlying the charge-trapping dielectric layer 404. It will be appreciated that any number of such wordlines can be formed over the dielectric layer 404, and that such wordlines may correspond to the wordlines 302 depicted in Fig. 3. The wordlines can be formed out of a polysilicon material, for example, where the polysilicon material may be deposited over the dielectric layer 404 and then patterned and etched.

Page 12, lines 30 - page 5, line 13: Please replace the paragraph with the following paragraph:

The first insulating layer can be formed to a thickness of about 70 Angstroms or less, for example, while the charge trapping layer can be formed to a thickness between about 60 to 80 Angstroms, for example. The second insulating layer can be formed to a thickness between about 100 to 200 Angstroms, for example. The second insulating layer is formed to a greater thickness relative to the other layers since it may be exposed to and altered by subsequent processing conditions. As set forth below, this layer may ultimately be stripped and re-applied at a desired (*e.g.*, lesser) thickness to re-establish uniformity and to facilitate desired device operation once particular processing has been completed. The second insulating layer may, accordingly, be referred to as a sacrificial oxide. In the above regard, since the top layer may act as a sacrificial layer, the layer need only be generally selective with respect to the spacer layer material to be described *infra* and then selective with respect to the underlying charge trapping layer so that ~~the~~ during its subsequent removal, the charge trapping layer will not be adversely damaged.